FPGA Synthesisable code of vending machine:-

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 15.04.2023 20:07:51

// Design Name:

// Module Name: vending\_machine

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

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// Dependencies:

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// Revision:

// Revision 0.01 - File Created

// Additional Comments:

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//////////////////////////////////////////////////////////////////////////////////

module vending\_machine(

input clock,rst,

input [3:0] in,

output reg[1:0] out,

output reg [3:0] change,

output reg [1:0] changehb

);

wire clk;

parameter s0= 4'b0000;//Rs.0

parameter s1= 4'b0001;//Rs.1

parameter s2= 4'b0010;//Rs.2

parameter s3= 4'b0011;

parameter s4= 4'b0100;

parameter s5= 4'b0101;//Rs.5

parameter s6= 4'b0110;

parameter s7= 4'b0111;

parameter s8= 4'b1000;

parameter s9= 4'b1001;

parameter m0= 2'b00; // No product dispersed

parameter m1= 2'b01; //Pepsi dispersed

parameter m2= 2'b10; //Coca Cola dispersed

parameter m3= 2'b11; //Maaza dispersed

reg[3:0] c\_state,n\_state;

userclock(clock,clk);

always@(posedge clk)

begin

if (rst==1)

begin

c\_state=0;

n\_state=0;

change=s0;

changehb=2'b00;

end

else

begin

c\_state=n\_state;

case(c\_state)

s0 : begin

if(in==s1)

begin

n\_state=s1;

out=m0;

change=s0;

end

else if(in==s2)

begin

n\_state=s6;

out=m0;

change=s0;

end

else if(in==s5)

begin

n\_state=s6;

out=m0;

change=s1;

changehb=2'b10;

end

else

begin

n\_state=s0;

out=m0;

change=s0;

end

end

s1:

begin

if(in==s1)

begin

n\_state=s6;

out=m0;

change=s0;

end

else if(in==s2)

begin

n\_state=s6;

out=m0;

change=s1;

end

else if(in==s5)

begin

n\_state=s6;

out=m0;

change=s2;

changehb=2’b10;

end

else if(in==s0)

begin

n\_state=s0;

out=m0;

change=s1;

end

else

begin

n\_state=s1;

out=m0;

change=s0;

end

end

s6:

begin

if(in==s7)

begin

n\_state=s0;

out=m1;

change=s0;

changehb=2'b00;

end

else if(in==s8)

begin

n\_state=s0;

out=m2;

change=s0;

changehb=2'b00;

end

else if(in==s9)

begin

n\_state=s0;

out=m3;

change=s0;

changehb=2'b00;

end

else if(in==s1)

begin

n\_state=s6;

out=m0;

change=s1;

changehb=2'b00;

end

else if(in==s2)

begin

n\_state=s6;

out=m0;

change=s2;

changehb=2'b00;

end

else if(in==s5)

begin

n\_state=s6;

out=m0;

change=s5;

changehb=2'b00;

end

else

begin

n\_state=s6;

out=m0;

change=s0;

changehb=2'b00;

end

end

default:

begin

n\_state=s0;

out=m0;

change=s0;

end

endcase

end

end

always @ (posedge clk)begin

if(out==2'b01)

$display("pepsi dispached");

else if(out==2'b10)

$display("cocacola dispached");

else if(out==2'b11)

$display("Maaza dispached");

end

endmodule

module userclock(input clock,output clk);

reg clk\_out=0;

reg [25:0] count=0;

always @(posedge clock)

begin

count<=count+1;

if (count==9500000)

begin

count<=0;

clk\_out=~clk\_out;

end

end

assign clk=clk\_out;

endmodule



